TSMC Property

# Foundry WLSI Technology for Power Management System Integration

**Chuei-Tang Wang, Chih-Lin Chen, Jeng-Shien Hsieh, Victor C.Y. Chang, Douglas Yu**

**R&D,TSMC**

**Oct. 2016**



Open Innovation Platform®

© 2016 TSMC, Ltd

# Outline

- **Motivation**
  - PMIC system integration trends
  - Foundry WLSI technology Portfolio
- **High Performance Computing System (HPC) on CoWoS**
  - VR on CoWoS
  - Impact of Si interposer
- **Mobile AP and PMIC System (MAPS) on InFO**
  - Power Delivery Network
  - PVR on InFO
- **Summary & Outlook**

TSMC Property

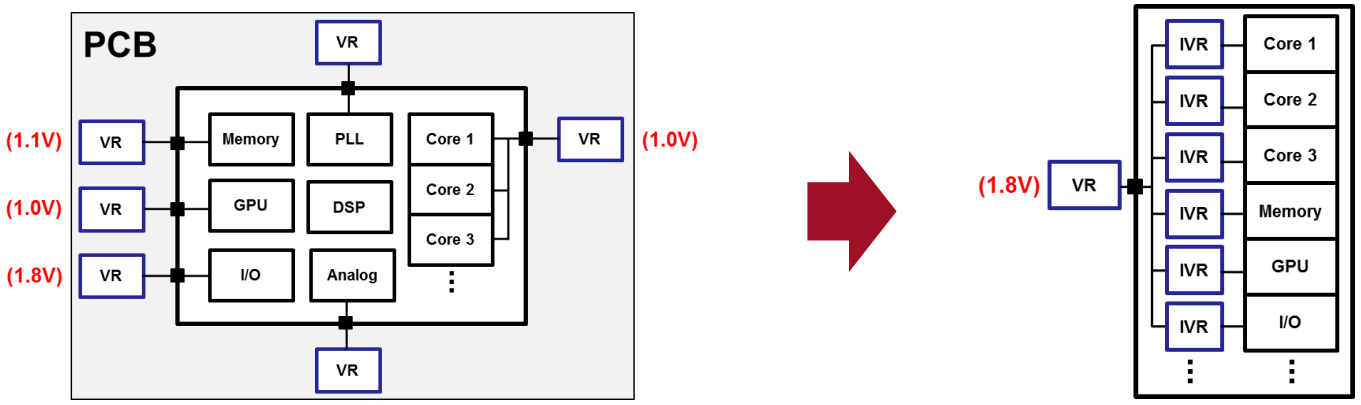


Open Innovation Platform®
© 2016 TSMC, Ltd

# Motivation: High Efficiency Power Management System

TSMC Property

- **PMIC System Trend:**
  - System on PCB → System on SoC/Package
  - Shared Voltage → Per-core Voltage Control
  - $V_{dd}$ Scaling → Low PDN Impedance Needed
  - Long Battery Life → High Efficiency Voltage Regulator
- **System on PCB → System on SoC/Package**



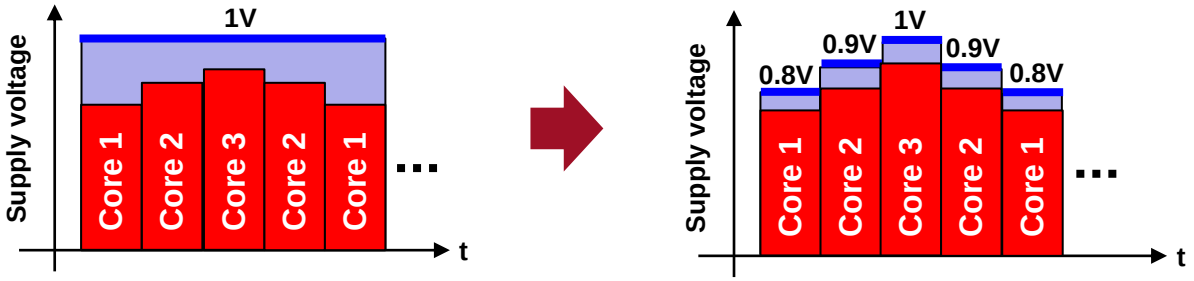



© 2016 TSMC, Ltd

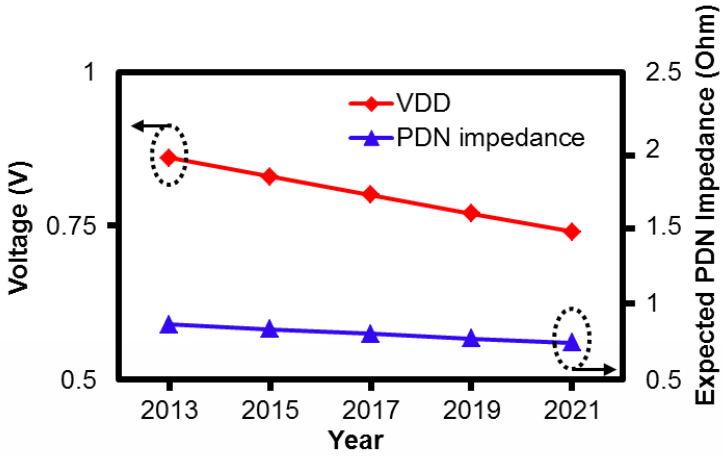
# Motivation: High Efficiency Power Management System

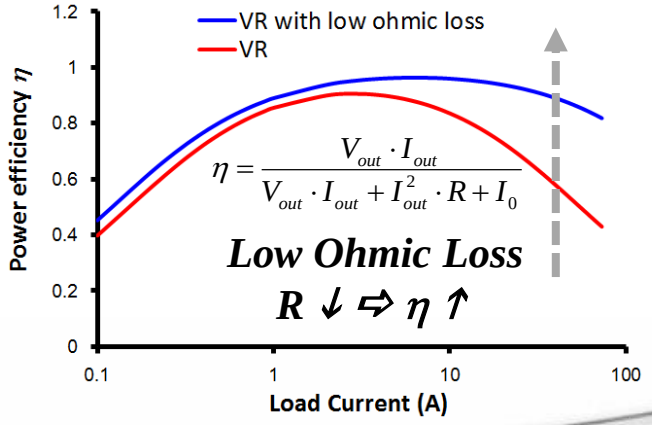
TSMC Property

- **Shared voltage → Per-core voltage control**




- **$V_{dd}$ Scaling → 0.74V → Low PDN Impedance**
- **Long Battery Life → High Efficiency VR → Low Ohmic Loss**



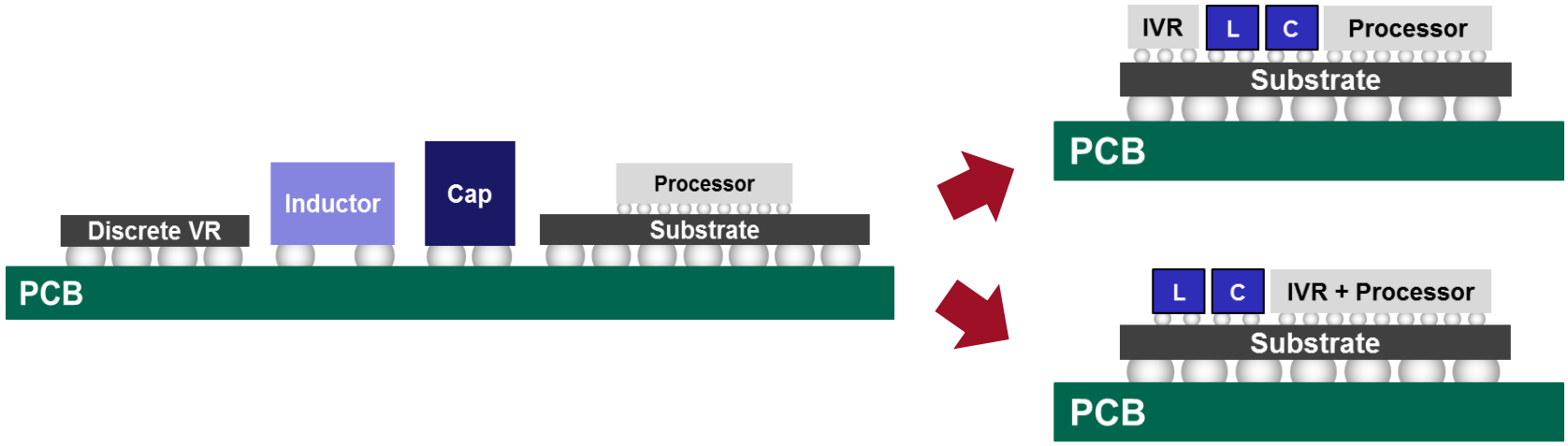

Source: 2013 ITRS & JEDEC



Open Innovation Platform®
© 2016 TSMC, Ltd

# System Integration from PCB to Package

TSMC Property




- **Benefits from System on Package**
  - PDN path: Long → Short
  - Discrete component number: Dozen → Several
  - Switching frequency: 10 MHz → 100 MHz
    - L: μH → nH
    - C: μF → nF
  - Form factor: Large → Small



© 2016 TSMC, Ltd

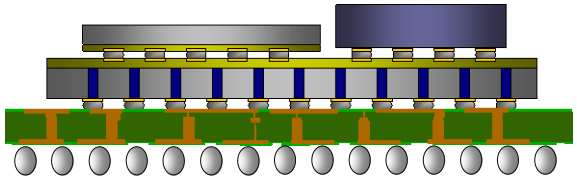
TSMC Property

# TSMC WLSI Technology Platforms
## from low cost to high performance

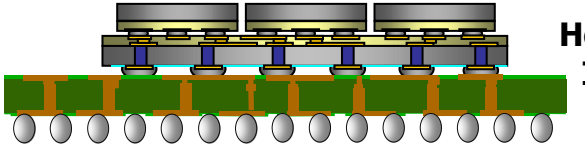
IO # to Substrate or PCB

PKG Size ($mm^2$)

**Heterogeneous Integration**

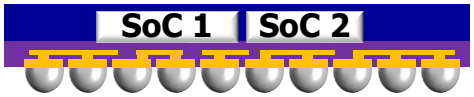


**Homogeneous Integration**

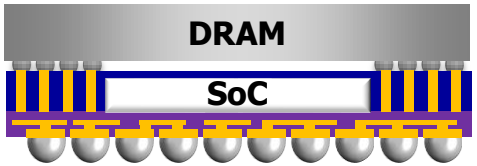


***InFO***

Multi-chip integration
3D integration
Smallest form factor
Cost competitive




**InFO_PoP**




***CoWoS®***

High performance and bandwidth
Multi-chip integration
Flexible integration

*** WLSI: Wafer Level System Integration**

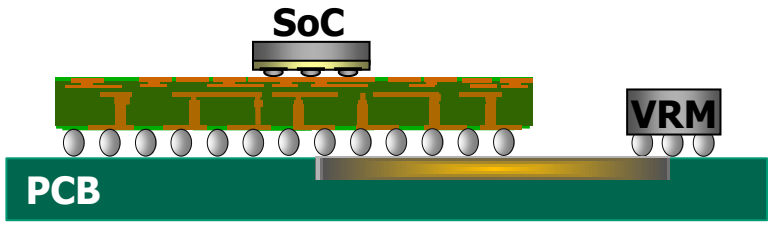


© 2016 TSMC, Ltd

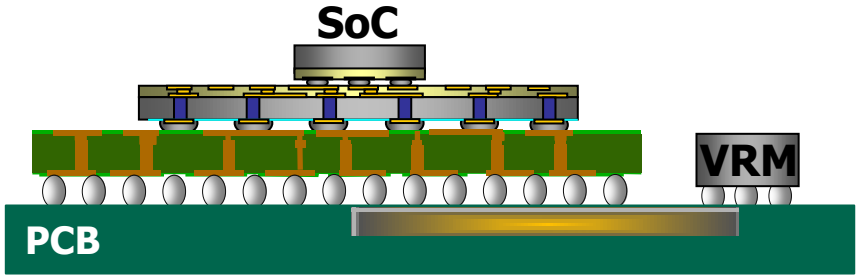
# SoC and VR(M) System Design on CoWoS

TSMC Property

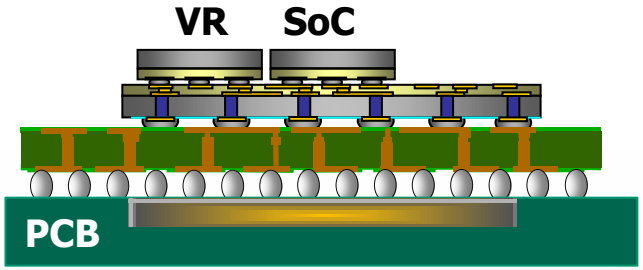
- System 1: VRM on board, SoC on substrate (FCBGA)




- System 2: VRM on board, SoC on Si interposer




- System 3: VR and SoC on Si interposer

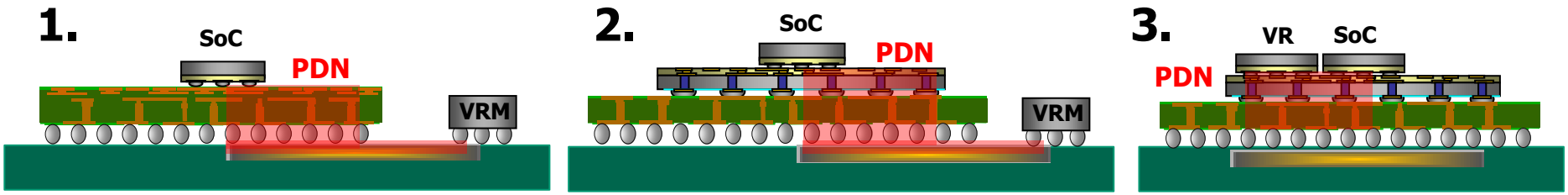





Open Innovation Platform®
© 2016 TSMC, Ltd

# SoC and VR(M) System Design on CoWoS

TSMC Property



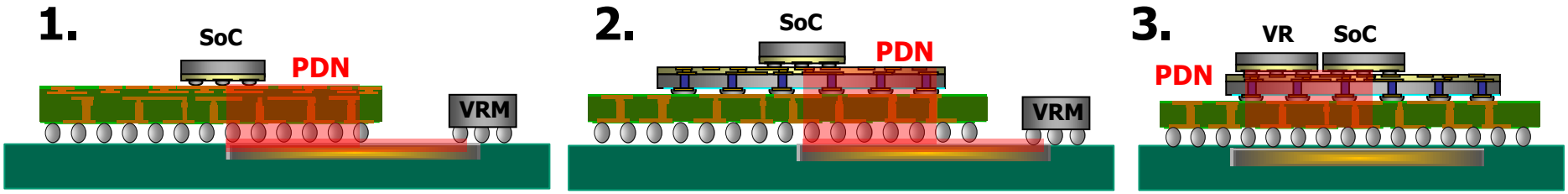

- **System 1: VRM on board, SoC on substrate**
  - PDN path: VRM → PCB → Substrate → SoC
  - PDN L/W: PCB/50/5 mm, Substrate/12/4 mm
  - PDN metal layer: PCB/2, Substrate/10
- **System 2: VRM on board, SoC on Si interposer**
  - PDN path: VRM → PCB → Substrate → Si Interposer → SoC
  - PDN L/W: PCB/50/5 mm, Substrate/12/4 mm, Si interposer/12/4 mm
  - PDN metal layer: PCB/2, Substrate/8, Si Interposer /2
- **System 3: VR and SoC on Si interposer**
  - PDN path: VR → Si Interposer and Substrate → SoC
  - PDN L/W: Substrate/12/4 mm, Si interposer/12/4 mm
  - PDN metal layer: Substrate/8, Si Interposer /2
- **FOM: PDN impedance, voltage drop and voltage variation**

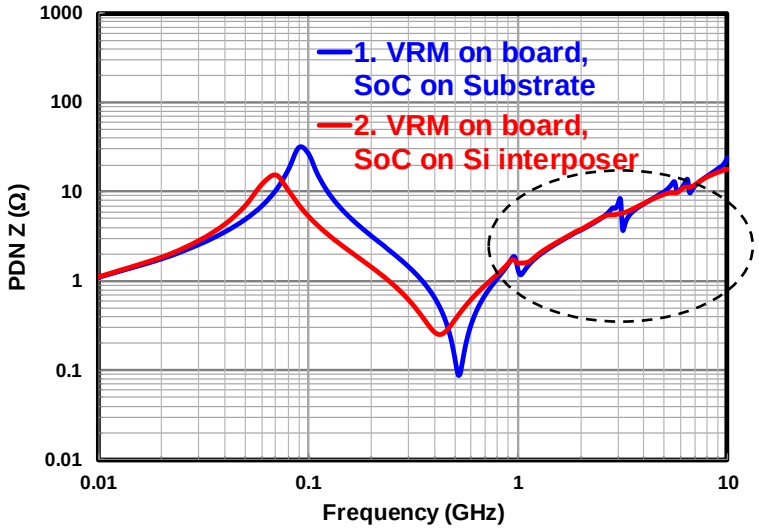


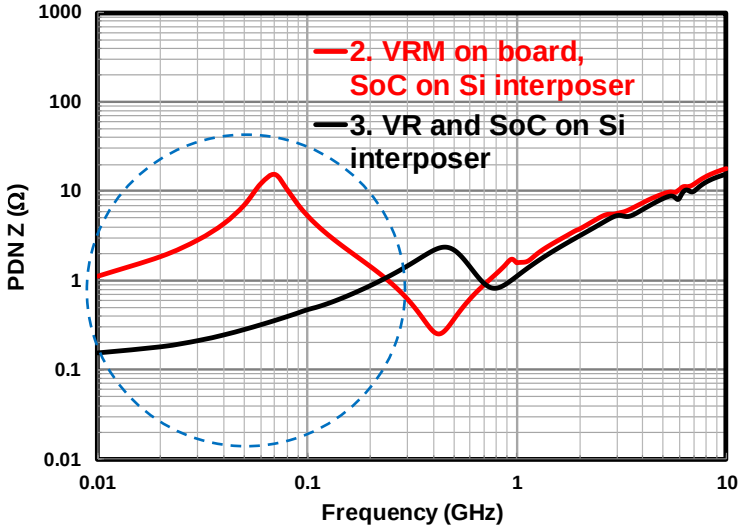
© 2016 TSMC, Ltd

# PDN Impedance Reduction from Si Interposer

TSMC Property




**Interposer mitigates anti-resonance at high frequencies**

**Short interconnect reduces PDN impedance: DC and AC**

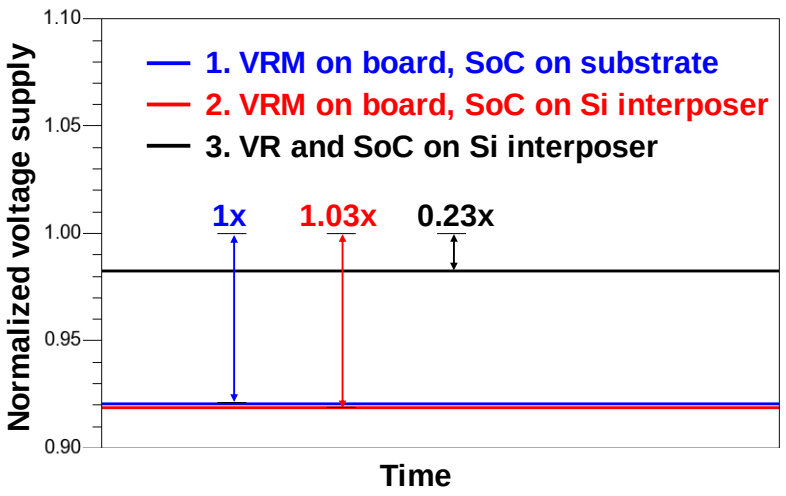
**Numbers of De-cap to be decreased**



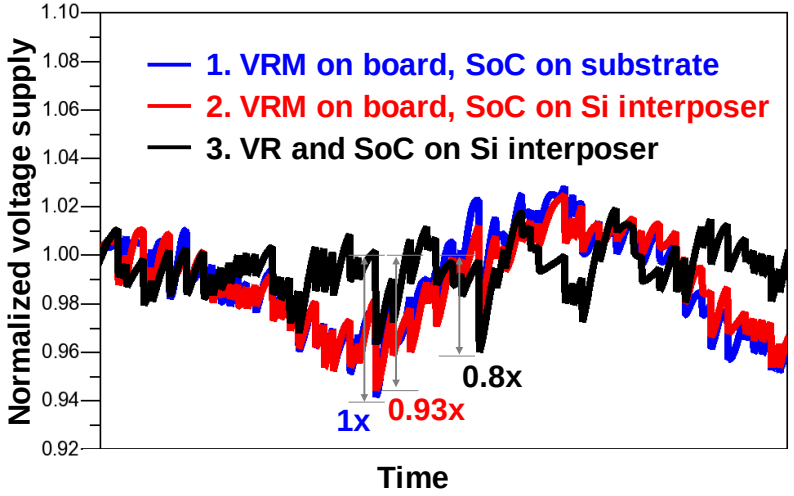
© 2016 TSMC, Ltd

# Si Interposer Reduces Voltage Drop and Voltage Variation

TSMC Property




**DC voltage drop**




**Voltage variation**
**(@ 2GHz switching freq.)**

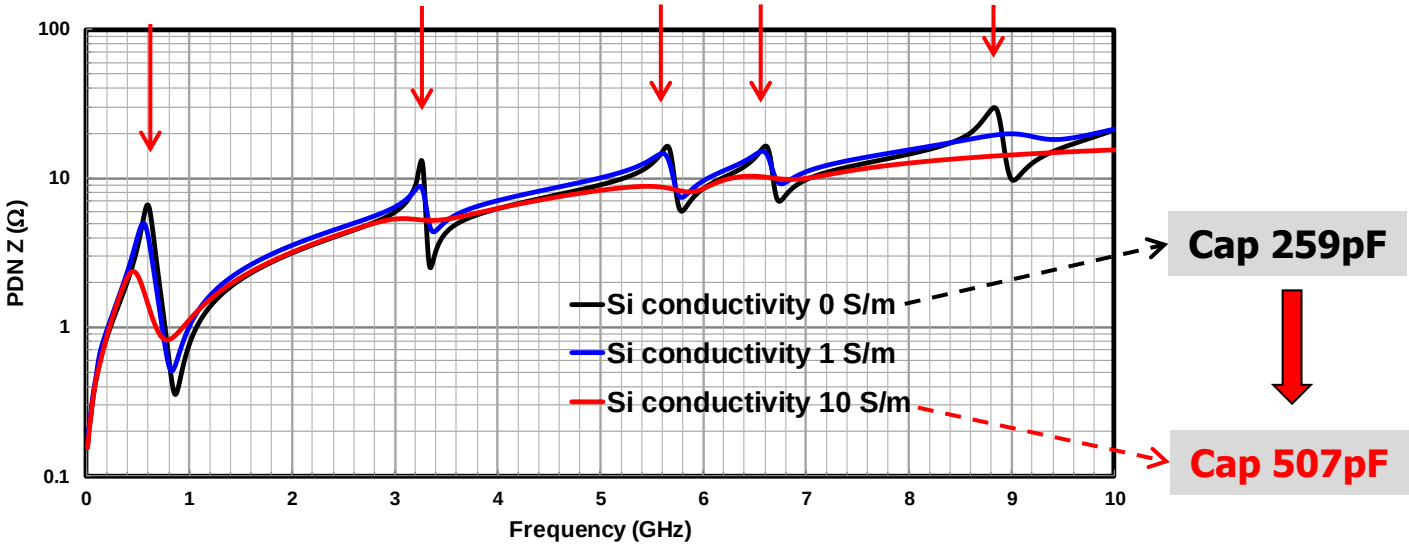
- **The voltage drop and voltage variation from VR to SoC ∝ PDN Impedance**
- **The VR and SoC on Si interposer system**
  - DC voltage drop: 23% of VRM on board, SoC on substrate system
  - Voltage variation: 80% of VRM on board, SoC on substrate system



© 2016 TSMC, Ltd

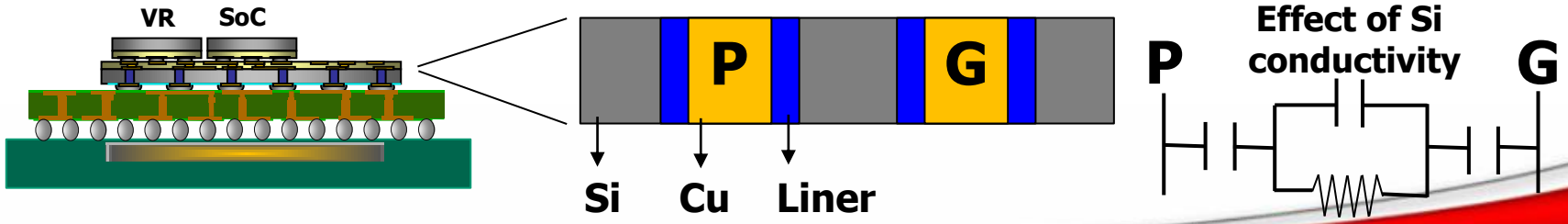
TSMC Property

# Capacitance of Si Interposer Suppresses PDN Z Anti-Resonances




- High conductivity Si interposer suppresses the anti-resonances
- High Si conductivity → High TSV Liner capacitance → More suppression of PDN Z anti-resonance

## Cross section of TSV and equivalent circuits

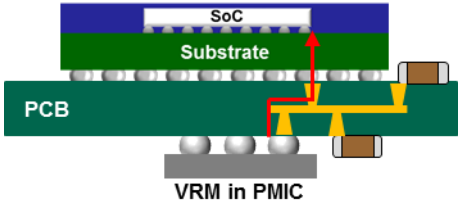




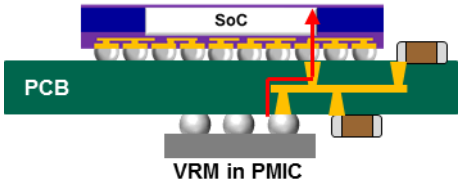

© 2016 TSMC, Ltd

# SoC and VR(M) System Design on InFO for Mobile Products

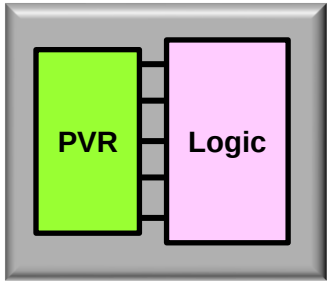
TSMC Property




System 1: FC and PMIC




System 2: InFO and PMIC




InFO and FC PKG

System 3: InFO with PVR

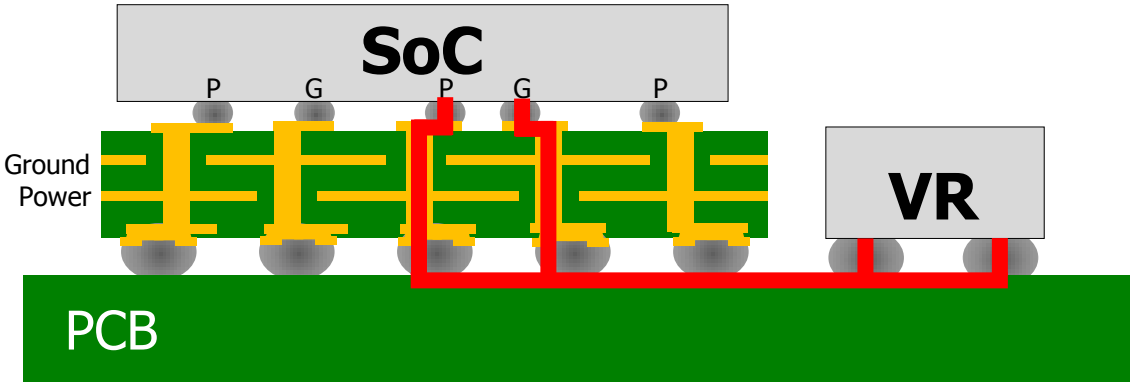
- **System 1: FC and PMIC**
  - PDN path: VRM → PCB → Substrate → SoC
  - PDN routing: in millimeter scale
- **System 2: InFO and PMIC**
  - PDN path: VRM → PCB → InFO→ SoC
  - PDN routing: in millimeter scale
- **System 3: InFO with partitioned VR (PVR)**
  - PDN path: VR → InFO→ SoC
  - PDN routing: in micrometer scale
- **FOM: PDN impedance, voltage drop, voltage variation, power response**



© 2016 TSMC, Ltd

TSMC Property

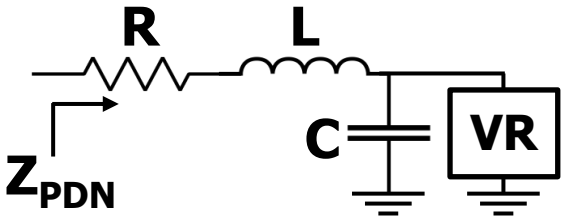
# Power Integrity – PDN Impedance Calculation




- PI: A measure for power supply stability; related to impedance of power distribution network (PDN)
- PDN impedance is

$$Z_{PDN} = R + j\omega L + \left(\frac{1}{j\omega C} \,//\, Z_{VR}\right)$$

where $Z_{VR}$ is the impedance of voltage regulator.



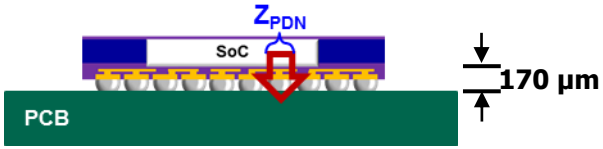

- Low R & L in PDN → Low $Z_{PDN}$ → Better PI performance



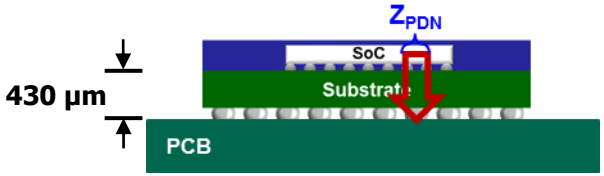
© 2016 TSMC, Ltd

# Low PDN Impedance in InFO Package

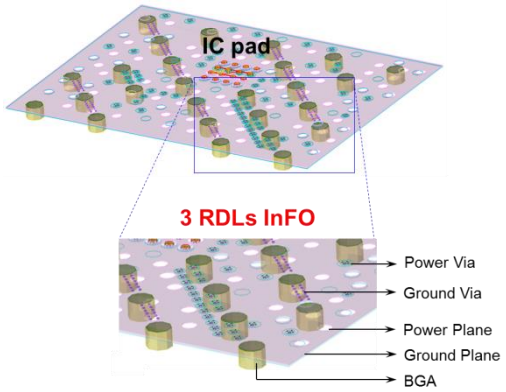
TSMC Property

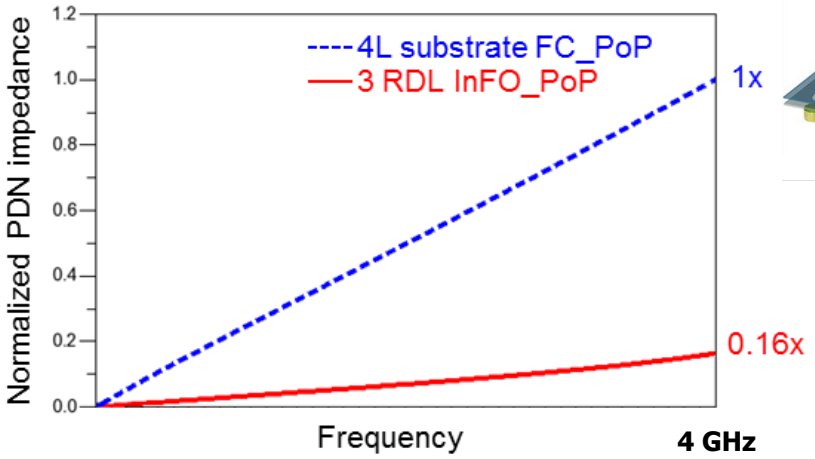


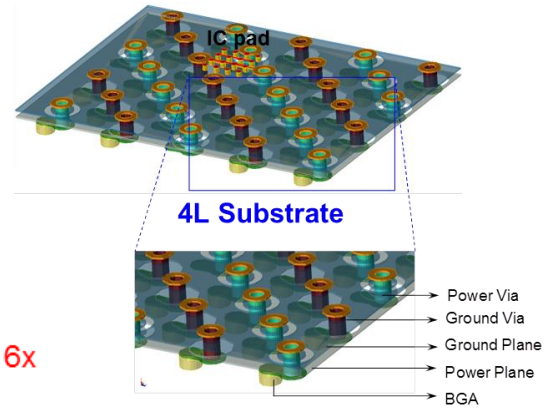

3 RDLs InFO




4L Substrate FC



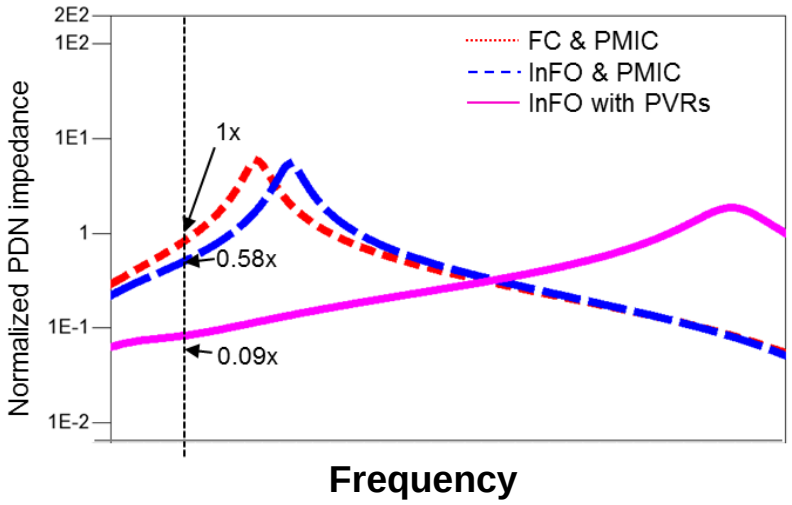

- PDN impedance: InFO_PoP is 16% of the FC_PoP.
- InFO_PoP: Substrate & C4 Bump eliminated and thin RDL
- Low PDN impedance → High power stability



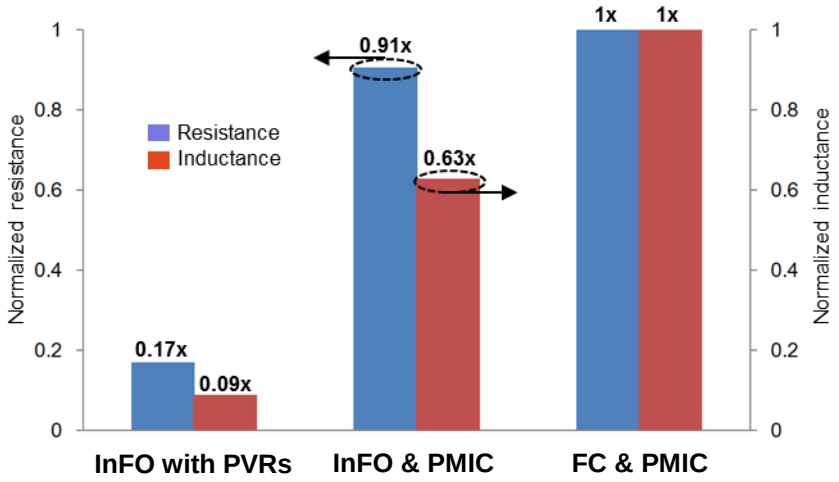
© 2016 TSMC, Ltd

# The PDN Impedance for the InFO + PVRs system

TSMC Property




**PDN impedance**




**Resistance and Inductance**

## InFO with PVRs system

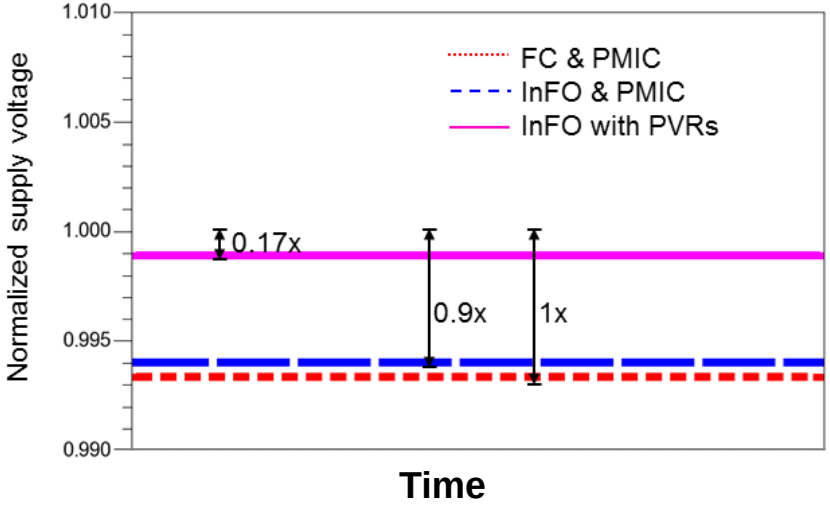
- PDN impedance: 9% of FC & PMIC system
- Resistance: 17% of FC & PMIC system
- Inductance: 9% of FC & PMIC system



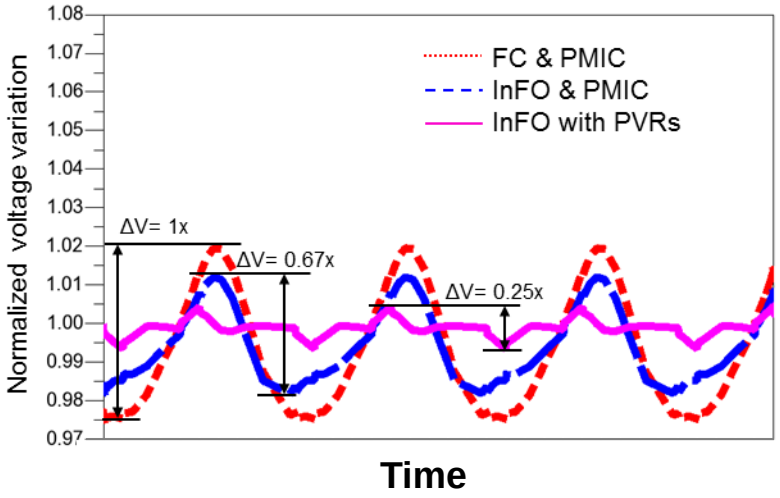
© 2016 TSMC, Ltd

TSMC Property

# The Voltage Drop and Variation for the InFO + PVRs System




**DC voltage drop**




**Voltage variation (ΔV)**

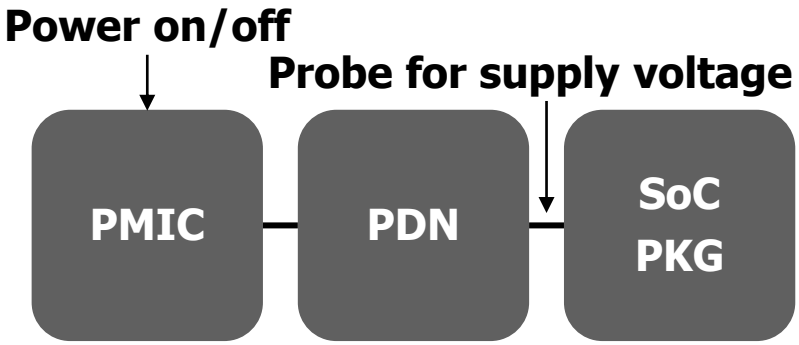
- **The voltage drop and voltage variation from VR to AP ∝ PDN Impedance**
- **The InFO with PVRs system**
  - DC voltage drop: 17% of FC & PMIC system
  - Voltage variation: 25% of FC & PMIC system

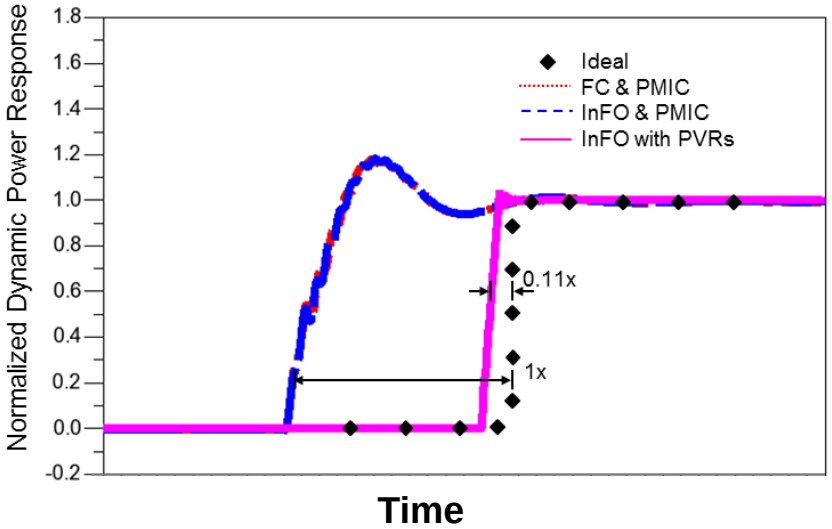


© 2016 TSMC, Ltd

# Power Response for InFO + PVRs System

TSMC Property




**Dynamic power response**

- **Transient time: Time period for power on from 0 to 1 stable state**
- **The InFO with PVRs system**
  - Transient time: 11% of FC & PMIC system



© 2016 TSMC, Ltd

# Summary of the PI Results

TSMC Property

| System specifications | PDN Z @10MHz | PDN Z @200MHz | Voltage drop | Voltage variation |
|---|---|---|---|---|
| System 1: VRM on board, SoC on substrate (FCBGA) | 1x | 1x | 1x | 1x |
| System 2: VRM on board, SoC on Si interposer | 1.01x | 0.45x | 1.03x | 0.93x |
| System 3: VR and SoC on Si interposer | 0.14x | 0.27x | 0.23x | 0.8x |

| System specifications | Resistance | Inductance | Voltage variation | Transient time |
|---|---|---|---|---|
| InFO with PVRs | 0.17x | 0.09x | 0.25x | 0.11x |
| InFO & PMIC | 0.91x | 0.63x | 0.67x | 1x |
| FC & PMIC | 1x | 1x | 1x | 1x |



© 2016 TSMC, Ltd

TSMC Property

# Summary and Outlooks

- **Foundry WLSI technology, CoWoS and InFO, provides leading edge solutions for power management system integration.**
- **The technologies provide excellent PDN performance for low power consumption, low voltage drop and low voltage variation for system design.**
- **$V_{dd}$ scaling of SoC leads to power system design challenges → TSMC WLSI technology provides the design solution.**



Open Innovation Platform®

© 2016 TSMC, Ltd

TSMC Property

# Thanks for your attention!



© 2016 TSMC, Ltd